Customer No.: 31561
Application No.: 10/710,301
Docket No.: 11574-US-PA

REMARKS

Present Status of Application

The Office Action dated December 14, 2004, objected claim 5 for informalities. Claims 1-3, 5 and 6 were rejected under 35 USC§102(a) as being anticipated by Nagano et al. (US Patent No. 6,441,420). Claim 4 was rejected under 35 USC§103(a) as being unpatentable over Nagano et al. and in view of Heida et al. (US Patent No. 6,777,776). Claim 7 was rejected under 35 USC§103(a) as being unpatentable over Nagano et al. and in view of Rinne et al. (US Publication No. 2002/0020551 A1).

Claims 1 and 5 have been amended for correcting informalities and providing more descriptions. Figure 2 has been amended to correct the mislabeled reference numbers. Submitted for the Examiner's approval is the formal copy of the proposed drawing (Fig. 2) including proper labeling. No new matter has been added to the application by the amendments made to the specification, claims and drawings. This Amendment is promptly filed to place the above-captioned case in condition for allowance. After entering the amendments and considering the following discussions, a notice of allowance is respectfully solicited.

Discussion for the objections

Claim 5 was objected for informalities.

In response to this objection, claim 5 has been amended to provide proper antecedent basis.

Withdrawal of this objection is respectfully requested.

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Discussion for 35 USC§102 and 103 rejections

Claims 1-3, 5 and 6 were rejected under 35 USC§102(a) as being anticipated by Nagano et al. (US Patent No. 6,441,420). Claim 4 was rejected under 35 USC§103(a) as being unpatentable over Nagano et al. and in view of Heida et al. (US Patent No. 6,777,776). Claim 7 was rejected under 35 USC§103(a) as being unpatentable over Nagano et al. and in view of Rinne et al. (US Publication No. 2002/0020551 A1).

The Office Action considered that Nagano et al. substantially disclosed this invention.

Claim 1 has been amended to provide more descriptions for clarification purposes, according to the present invention. Supporting grounds for this amendment can be found at least in figure 1 and the related descriptions in the specification.

Applicants submit that amended independent claim 1 patently defines over the prior references for at least the reason that the cited art fails to disclose each and every feature as claimed in the present invention.

The independent claim 1 recites:

1. A wafer level passive component, suitable for a chip, the chip at least having an active surface, a first contact pad, a second contact pad and a passivation layer, the first contact pad and the second contact pad disposed on the active surface, the passivation layer disposed on the active surface and exposing the first contact pad and the second contact pad, the wafer level passive component at least comprising:

a first conductive pattern, lying over the active surface and having a first connecting area and a first overlapping area, wherein the first connecting area physically connects to the first contact pad and the first overlapping area lies on the passivation layer;

a dielectric pattern, lying on the first overlapping area of the first conductive pattern; and

a second conductive pattern, lying over the active surface and having a second connecting area and a second overlapping area, wherein the second connecting area physically connects to the second contact pad, the second overlapping area lies on the

dielectric pattern, and at least a portion of the dielectric pattern is interposed between the first overlapping area and the second overlapping area.

Applicant respectfully asserts that claim 1 is patentably distinct from the prior art structures, especially at least the first connecting area physically connects to the first contact pad and the first overlapping area lies on the passivation layer, as well as the second connecting area physically connects to the second contact pad, the second overlapping area lies on the dielectric pattern, and at least a portion of the dielectric pattern is interposed between the first overlapping area and the second overlapping area.

Nagano discloses a substrate 100 including impurity diffusion layers 105 as source/drain regions of the FET transistors. The protective film 106 is deposited over the substrate 100 and contact plugs 107 and 108 in the protective film 106 are connected to the impurity diffusion layers 105. Nagano also teaches a plurality of lower electrodes 109 each connected to the contact plug 107, the capacitor insulating film 110A over the lower electrodes 109 and an upper electrode 111 connected to the contact plug 108.

The Office Action considered Nagano's impurity diffusion layers 105, lower electrodes 109 and upper electrode 111 being respectively comparable to the contact pads, the first conductive pattern and the second conductive pattern of this application. Applicant respectfully disagrees with this consideration.

At first, as taught by Nagano, the impurity diffusion layers 105 serve as the source/drain regions of the FET transistors, which function very differently from the contact pads and should not be considered comparable to the contact pads. Even if considering Nagano's impurity diffusion layers 105 being comparable to the contact pads

of this invention, Nagano fails to teach or suggest the first and second conductive patterns, as recited in claim 1. Nagano's lower/upper electrode 109/110 are not physically connected to impurity diffusion layer 105, but physically connected to the contact plugs 107/108. Also, Nagano fails to disclose the dielectric pattern, because Nagano's capacitor insulating film 110A is disposed on and covers the whole lower electrode 109, rather than only lying on the first overlapping area.

Accordingly, the structure of the present invention is patentably distinct from the prior art reference Nagano because Nagano fails to disclose all limitations of independent claim 1. As a result, Nagano did not anticipate the present invention as suggested by the Office Action, to arrive at the present invention as recited in independent claim 1. For at least the foregoing reasons, all pending claims patently define over the cited reference and should be allowed.

Consequently, reconsideration and withdrawal of these 102 rejections are respectfully requested.

Regarding claims 4 and 7, the Office Action further relied on Heida et al. or Rinne et al. respectivcly for teaching the dielectric pattern being aluminum oxide or the under bump metallurgy layer.

As discussed above, the structure of the present invention is patentably distinct from the prior art reference because Nagano fails to disclose all limitations of independent claim 1. However, either Heida or Rinne fails to remedy the deficiencies of Nagano. Therefore, it is respectfully submitted that claim 4 or 7 patentably distinguishes over the cited references, either alone or in combination, for at least the reasons stated above as

well as for the additional features that this claim recites.

Withdrawal of these rejections under 35 USC 103(a) is respectfully requested.

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CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date : March 14, 2005

Respectfully submitted,

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